AN INTERCONNECTION NETWORK FOR A FIELD PROGRAMMABLE GATE ARRAY

ABSTRACT OF THE DISCLOSURE

An interconnection network architecture which provides an interconnection network which is especially useful for FPGAs is described. Based upon Benes networks, the resulting network interconnect is rearrangeable so that routing between logic cell terminals is guaranteed. Upper limits on time delays for the network interconnect are defined and pipelining for high speed operation is easily implemented. The described network interconnect offers flexibility so that many design options are presented to best suit the desired application.